REMARKS

Claims 19-24 and 29 are pending in this application. Claims 19 and 22 are independent. By virtue of the present amendment, claim 23 is canceled, and claim 24 is amended to depend upon claim 22 rather than claim 23. Claims 19 and 22 are amended to correct informalities. No new matter has been introduced.

The Information Disclosure Statement is objected to for failure to fully comply with the requirements of 37 CFR 1.98(b). An amended copy of the June 18, 2007 Information Disclosure Statement was timely filed on December 6, 2007, adding the information requested by the Examiner. Applicants sincerely apologize for the mistakes and omissions in the June 18th Information Disclosure Statement and thank the Examiner for allowing us to amended this document.

Claim 23 stands rejected by the Examiner under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter of the invention.

Claims 19-21 and 29 stand rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over US Patent Number 4,063,220, issued to Robert M. Metcalf, *et al* on December 13, 1977 (hereafter "Metcalf"), in view of AMD's Am79C830 FORMAC Plus as disclosed in "The SUPERNET 2 family for FDDI – 1991/1992 World Network Data Book" (hereafter "AMD") in further view of Donald O. Nessman and Pedro P. Rodriguez's teachings entitled "Using ASICs for Component Integration" (hereafter "Nessman").

Claim 22 stands rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over AMD in view of US Patent 5,774,640, issued to Kay M. Kurio on June 30, 1998 (hereafter "Kurio") in further view of US Patent 4,860,193, issued to Steven R. Bentley, *et al* on August 22, 1989 (hereafter "Bentley").

Claims 23 and 24 stand rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over AMD in view of Kurio in further view of Bentley

and in further view of US Patent Number 5,210,749 (for claims 23-24), issued to Farzin Firoozman, *et al* on May 11, 1993 (hereafter "Firoozman").

35 U.S.C. § 112 rejection is moot

Claim 23 stands rejected by the Examiner under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter of the invention. Claim 23 has been canceled. This rejection is moot.

AMD, Metcalf, Nessman do not teach early interrupt of host

Claims 19-21 and 29 stand rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over Metcalf in view of AMD and Nessman. Applicants respectfully traverse this rejection for several reasons.

First of all, claims 19-21 and 29 recite an adaptor "for generating a receive interrupt signalling to said host computer that data has been received by said transceiver, wherein said data receive control circuitry is operative to generate said receive interrupt once said transceiver has received over said communications media a predetermined number of bytes of a data packet." The "interrupt...to said host...once...transceiver has received...a predetermined number of bytes..." is not taught by AMD, Metcalf, nor Nessman.

Metcalf teaches general Ethernet and Nessman teaches ASICs, so the Office Action looks to AMD for this element. However, AMD does not teach an interrupt of the Host. The AMD architecture is complex, and includes several chips to handle the processing of the FDDI packets. In addition to the FORMAC chip, there are buffer memory chips and a Node Processor (NP) to handle some aspects of the protocol. See the diagrams in AMD on pages 2-4 and 1-1. The Node Processor and its functionality are described on page 1-3:

> **Node Processor**
>
> The Node Processor (NP) can be a microprogrammed or conventional microprocessor-based system used for overseeing the operation of the SUPERNET 2 chip-set. Its main function is to initialize the devices and respond to various system-level and frame-level interrupts. In the simplest case it can be a minimal state machine. More complex architectures can have all the sophistication required to execute the upper-layer protocols specified by the seven-layer International Standards Organization (ISO) Open System Interface (OSI) model.

It is important to note that AMD teaches that the Node Processor handles the interrupts from the FORMAC chip. These interrupts are not sent to the host, as is specified in claims 19-21 and 29.

In the teachings of AMD at 2-21, there is a diagram of the signals generated by the FORMAC chip. Signals RDATA, HSACK, HSREQ2-0 and QCTRL2-0 are addressed to the host. The HSACK, HSREQ2-0 and the QCTRL2-0 signals are used to coordinate the synchronization of reading and writing data from the queues in buffer memory. The RDATA signal is used to tell the host that data in the buffer memory is ready to be transferred to the host. There is no indication that any of these signals are used as an interrupt to the host.

The Office Action cites to MINTR1 and MINTR2 as interrupts. However, these interrupts are destined to the Node Processor and not to the Host. See AMD at page 2-21, where MINTR1 and MINTR2 are directed to the NP. Because MINTR1 and MINTR2 are directed to the processor that handles initialization and protocol related (as opposed to data related) processing, they can not be used to signal information on the amount of data received.

Since the interrupts from the FORMAC are not directed to the host, the "...interrupt signal to said host computer..." of claims 19-21 and 29 are not found in AMD, Metcalf, not Nessman, and the rejection under 35 U.S.C. § 103(a) can not be sustained.

AMD, Metcalf, Nessman do not teach a single ASIC

Furthermore, claims 19-21 and 29 recite a device "wherein said ethernet control circuitry, said host interface circuitry, and said data receive control circuitry, said data transmit control circuitry, said receive data buffer and said transmit data buffer are all contained in a single Application Specific Integrated Circuit (ASIC)." This claims that "all [are] contained in a single [ASIC]."

This is different from AMD. In AMD, the buffer memory is contained in a separate device and is not contained within the ASIC. See the Block Diagram in AMD at 1-1, 1-6, and numerous other locations within AMD.

There is no discussion in Metcalf of including the buffer memory in the ASIC either, so this element of claims 19-21 can not be found in the combination of Metcalf and AMD. As a result, the rejection under 35 U.S.C. § 103(a) can not be sustained.

In the most recent Office Action, the Examiner agreed with the above analysis, and looked to Nessman to teach the combination of the functionality in a single ASIC. However, a close reading of Nessman shows that he does not teach the use of a single ASIC, but in places teaches against a fully integrated ASIC. Nessman figure 2 teaches a "conventional system" with 6 chips (microprocessor, memory, 4 ASICs, and 24 discretes) compared to an "integrated system" with 3 chips (microprocessor, memory, 1 ASIC, and 12 discretes). There are no teachings in Nessman of placing the host interface circuitry, the data receive control circuitry, the data receive control circuitry and the data buffers into the ASIC.

Instead, Nessman teaches against the full integration as claimed in claim 19-21 and 29. Look to the sixth paragraph on page 697:

> **The desired level of component integration is determined through the examination of system requirements such as volume, performance, reliability and cost goals. The level of integration is subject to technical and economic limitations on chip complexity. Limitations involving both technical and economic issues result from the constraints of process, design, assembly and test of ASICs. In addition, consideration of the economic return on investment, generally favors the use of ASICs for products produced in high volume, where the initial cost of ASIC development is small compared to the total value of the systems produced.**

Nessman at pages 695 and 696 list a large number of limitations on the number of functions that can be combined in an ASICs. Given that this Nessman is used in combination with AMD, a particularly complex set of functionality, then this is teaching away from the Applicants single ASIC implementation of low level Ethernet functionality. This is teaching against the invention claimed in claims 19-21 and 29.

No motivation to combine AMD, Metcalf, and/or Nessman

In addition, there is no motivation to combine AMD with Metcalf and Nessman. AMD never mentions Ethernet and Metcalf never mentions FDDI. These are two independent and distinct protocols, with no motivation to combine or to exchange technologies. And Nessman never mentions Ethernet, FDDI or any other communications functionality. AMD teaches against the inclusion of all of the functions in a single ASIC. See AMD at the first paragraph of page 1-2: "The 4-chip

SUPERNET 2 family implements the FDDI standards..." A person of ordinary skill in the art would not combine AMD with Metcalf.

Furthermore, the SUPERNET implementation required a Node Processor, an additional chip. AMD again teaches against the single ASIC solution on page 1-3 in the last three paragraphs, where AMD teaches that "In the simplest case it can be a minimal state machine." It further teaches "The Node Processor (NP) can be a microprogrammed or conventional microprocessor based system..." By teaching the flexibility of using multiple options of the Node Processor, it teaches against the fixed solution of the ASIC in claims 19-21 and 29.

Therefore, the rejection of claims 19-21, and 29 under 35 U.S.C. § 103(a) can not be sustained.

AMD, Kurio, and Bentley do not teach multiple interrupts

Claims 22 and 24 stand rejected by the Examiner under 35 U.S.C. § 103(a) as being unpatentable over AMD in view of Kurio in further view of Bentley. Applicants respectfully traverse this rejection.

First of all, the Office Action fails to show multiple interrupts per incoming packet, as described in claims 22 and 24: "generating a first early receive interrupt from said adapter to said host computer;...thereafter generating a second early receive interrupt from said adapter to said host computer..." The Office Action cites to a single interrupt in AMD on page 2-64 column 1 (see above for a discussion of why this interrupt is not analogous to the claimed interrupt). But there is no second interrupt in AMD. Nor in Metcalf. Nor in Kurio. This element is missing, and the rejection under 35 U.S.C. § 103(a) can not be sustained.

AMD, Kurio, and Bentley do not teach adjusting threshold according to length of incoming packet

Furthermore, the Office Action looks to Bentley to provide the "adjusting said receive threshold according to said length of said packet." However, Bentley is misunderstood in the Office Action. Bentley teaches the use of the length of previously received packets to determine the threshold value. In the abstract of Bentley, the language is confusing, stating the subsequent block lengths are used to

calculate the threshold. It is clearer in Bentley, column 5 lines 6-12 where the algorithm is described:

> **In the preferred embodiment of the invention, the longest of the five consecutive data blocks is utilized as the C actual value for determining the new C threshold level. Obviously, in other data processing systems, other criteria can be established such as the average of a number of subsequent data block lengths or some statistical weighing technique.**

In either case, it is distinct from the term in claims 22 and 24 that calls for the use of the length of the incoming packet to set the threshold for the receipt of the remainder of that specific packet. Neither Bentley, AMD, nor Kurio discuss this aspect of claims 22 and 24.

As such, the combination of Bentley, AMD, and Kurio does not provide all of the elements of claims 22 and 24, and the rejection can not be sustained.

No motivation to combine AMD with Bentley and/or Kurio

Fourth, Bentley can not properly be combined with AMD because Bentley is used in a different field. Bentley describes the internal bus architecture of a computer system, and is not in the field of communications. AMD discusses the FDDI communications protocol. It is therefore highly unlikely that one ordinarily skilled in the art using AMD would know about Bentley, without the instruction of the present patent application.

Kurio is also distinct from Bentley and AMD. Kurio is related to fault tolerant computing and creating network interfaces to fault tolerant computers. It is unlikely that one ordinarily skilled in the art would look to a fault tolerant computer patent along with an internal bus architecture patent and a communications patent to derive the invention described in claims 22 and 24.

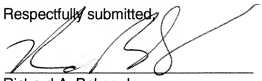
Applicants respectfully request that the Examiner remove the rejection to claims 22 and 24 under 35 U.S.C. § 103(a).

CONCLUSION

The pending claims define subject matter that is patentable, even in light of AMD, Metcalf, Bentley, Firoozman, and Kurio. The application is in condition for allowance. Applicants respectfully request prompt issuance of this application.

The commissioner is authorized to charge deposit account 503650 for any fees associated herein.

Respectfully submitted,



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